ABSTRACT

A bus device comprises a clock generator that is adapted to generate a clock signal for internal use by the bus device, data synchronizing logic that is adapted to synchronize source synchronous data that the bus device receives from the bus to the bus device's clock signal, and error detection and correction logic coupled to the data synchronizing logic. The error detection and correction logic is adapted to detect and correct errors associated with the data received from the bus concurrently while the data synchronizing logic synchronizes source synchronous data received from the bus to the clock signal.